CLAIM AMENDMENT

Please amend claims 29, 36 and add claims 38-44.

Claims 1-20 (cancelled).

Claim 21 (withdrawn): A method for manufacturing a semiconductor device, comprising,

preparing a semiconductor substrate having a grid-line area and a chip area, the chip area having a circuit area and a dummy area surrounding the circuit area;

forming a conductivity layer on the semiconductor substrate;

forming circuit patterns in the circuit area and a dummy pattern encompassing the circuit area in the dummy area by etching the conductivity layer;

forming a first insulating layer formed on an entire surface of the semiconductor substrate;

forming a second insulating layer formed only on the first insulating layer which is formed on the semiconductor substrate and on the circuit patterns;

forming a third insulating layer formed on the exposed first insulating layer and the second insulating layer; and

removing the first, second and third insulating layers in the grid-line area.

Claim 22 (withdrawn): A method for manufacturing a semiconductor device as claimed in claim 21, wherein the second insulating layer is formed by a SOG method.

Claim 23 (withdrawn): A method for manufacturing a semiconductor device, comprising,

preparing a semiconductor substrate having a grid-line area and a chip area, the chip area having a circuit area and a dummy area surrounding the circuit area;

forming a conductivity layer on the semiconductor substrate;

forming circuit patterns in the circuit area and a dummy pattern encompassing the circuit area in the dummy area by etching the conductivity layer;

forming a first insulating layer formed on an entire surface of the semiconductor substrate;

forming a second insulating layer on the first insulating layer;

removing the second insulating layer which is formed on the first insulating layer on the dummy pattern until the surface of the first insulating layer is exposed;

forming a third insulating layer formed on the exposed first insulating layer and on the second insulating layer; and

removing the first, second and third insulating layers in the grid-line area.

Claim 24 (withdrawn): A method for manufacturing a semiconductor device as claimed in claim 23, wherein the second insulating layer is formed by a SOG method.

Claim 25 (withdrawn): A method for manufacturing a semiconductor device as claimed in claim 23, wherein the second insulating layer is removed by a RIE method.

Claim 26 (withdrawn): A method for manufacturing a semiconductor device as claimed in claim 23, wherein the second insulating layer is a multi-SOG layer.

Claim 27 and 28 (cancelled).

Claim 29 (currently amended): A semiconductor device, comprising:

a semiconductor substrate having a first area where an integrated circuit is formed, a second area having a first part and a second part, and a third area where a pad pattern is formed, wherein the second area encompasses the first and third area;

wiring patterns formed on the substrate in the a first area;

a first dummy pattern which is formed of the same material as the wiring patterns, formed in the first part of the second area, ~~which is a first part~~ wherein the first part is located along an edge of the semiconductor substrate;

a second dummy pattern, which is formed of the same material as the wiring patterns, which is formed in the second part of the second area, ~~which is~~ wherein a second part is located between the first and the third areas, ~~and which is connected to the first dummy pattern~~ the first and the second dummy patterns being formed as a single integral structure, whereby [[a]] the pad pattern is encompassed by the first and second dummy patterns;

a second insulating layer formed over the wiring patterns and the first and second dummy patterns, an edge of the [[first]] second insulating layer being located on the pad pattern, which is adjacent the first and second dummy patterns; and

a first insulating layer formed above the semiconductor substrate, the first insulating layer being formed outside the first and second dummy patterns but not being formed over the first and second dummy patterns.

Claims 30-33 (canceled).

Claim 34 (previously presented): A semiconductor device as claimed in claim 29, wherein the first insulating layer has a moisture absorbable characteristic.

Claim 35 (previously presented): A semiconductor device as claimed in claim 29, wherein the first insulating layer is an SOG layer.

Claim 36 (currently amended): A semiconductor device as claimed in claim 29, wherein the first dummy pattern has a width, which is fixed by a concentration of solid content of the first insulating layer.

Claim 37 (previously presented): A semiconductor device as claimed in claim 29, further comprising a third insulating layer formed on the substrate, the first insulating layer being located between the second insulating layer and the third insulating layer.

Claim 38 (new): A semiconductor device as claimed in claim 29, wherein the width of the first dummy pattern is approximately 1 μm.

Claim 39 (new): A semiconductor device as claimed in claim 29, wherein the width of the second dummy pattern is approximately 1 μm.

Claim 40 (new): A semiconductor device as claimed in claim 38, wherein the width of the second dummy pattern is approximately 1 μm.

Claim 41 (new): A semiconductor device as claimed in claim 29, wherein the distance from the edge of the semiconductor substrate to the edge of the first dummy pattern is over 10 μm.

Claim 42 (new): A semiconductor device as claimed in claim 38, wherein the distance from the edge of the semiconductor substrate to the edge of the first dummy pattern is over 10 μm.

Claim 43 (new): A semiconductor device as claimed in claim 39, wherein the distance from the edge of the semiconductor substrate to the edge of the first dummy pattern is over 10 μm.

Claim 44 (new): A semiconductor device as claimed in claim 40, wherein the distance from the edge of the semiconductor substrate to the edge of the first dummy pattern is over 10 μm.